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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,985	04/19/2004	Shijian Luo	2269-5565.1US (02-1124.01)	3493
24247 TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110	7590 01/23/2007		EXAMINER STARK, JARRETT J	
			ART UNIT 2823	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/23/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

# Office Action Summary

Application No.

10/826,985

Applicant(s)

LUO ET AL.

Examiner

Jarrett J. Stark

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 12/11/2006 have been fully considered but they are not persuasive.

The Applicant's submitted "that Tong does not expressly or inherently describe healing cracks and delaminations produced during semiconductor dicing. Tong is silent as to whether or not cracks or delaminations in the initially cured B-stage material may be healed. Moreover, it is respectfully submitted that Tong does not describe circumstances in which an affirmative act of healing would occur, or conditions in which healing would inherently occur."

The examiner respectfully traverses this argument for the following reasons. As cited in the previous office action dated 9/7/2006, Tong teaches a dicing method that uses a semi-cured (B-stage) protective coating that receives a final curing step after the dicing step. Tong [0013] teaches that dicing the substrate while the (B-stage) protective coating is in its semi-cured stated ensures clean dicing of the wafer. Clean dicing of the wafer inherently means no chips or cracks.

It is further noted that Tong discloses all the limitations of the independent claim, except for the intended use recitation of specifically "healing" the cracks and delaminations, however since Tong is teaching the same method steps and use of the same materials, the method disclosed by Tong inherently is "healing" the cracks and delaminations. Thus, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order

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to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

**Claims 1-8 and 19-29** are rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (US 2003/0171456).

1. **Regarding claim 1**, Tong discloses a method for forming a protective layer on a plurality of semiconductor device components, comprising:

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providing a fabrication substrate carrying a plurality of semiconductor device components, adjacent semiconductor device components on the fabrication substrate being separated from one another by a street extending therebetween (Tong, ¶ [0013] – Inherently present before semiconductor chips or dies are separated/diced);

applying a protective material to active surfaces of at least the adjacent semiconductor device components (Tong, ¶ [0013] – B-stageable material – protective material that is semi-cured);

severing the protective material and at least partially severing the adjacent semiconductor device components from one another along the street (Tong, ¶ [0013] – Chips are dice after a being partially cured); and

healing cracks and delaminated areas in the protective material formed during the at least partially severing (Tong, ¶ [0013] – final complete curing).

In the preferred embodiment, the composition is B-stageable, i.e., the composition is capable of an initial solidification that produces a, smooth, non-tacky coating on the semiconductor wafer. The B-stage solidification preferably occurs in at a temperature in the range of about 100.degree. C. to about 150.degree. C. After the B-stage process, a smooth, non-tacky solid coating is obtained on the wafer to ensure the clean dicing of the wafer into individual chips. The final, complete curing occurs at a second temperature that is higher than the B-stage curing temperature. Generally, the final cure of the composition occurs after the formation of the interconnections. (Tong, ¶ [0013])

Structural Elements recited in the claim must manipulatively distinguish the claim from the prior art to have patentable weight.

“To be entitled to patentable weight in method claims, the recited structural limitations therein must affect the method in a manipulative sense and not amount to mere claiming of a use of a particular structure.”

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Ex parte Pfieffer, 135 USPQ 31,k 33 (Bd. Pat. App & Inter. 1961). Put another way, “patentability of a method claim must rest on the method steps recited, not on the structure used, unless that structure affects the method steps.” Leeson Corp. v. U.S., 185 USPQ 156, 165 (Ct. Cl. Trial div. 1975) aff’d 192 USPQ 672 (Ct. Cl 1976).

In Ex parte Pfieffer, 135 USPQ 31, 33 (Bd. Pat. App. & Inter. 1961) the claims set forth a method of dropping a rubber bag out of a airplane without the use of a parachute to transport free flowing material inside the bag to the ground. The applicant argued that the reference applied by the examiner did not use a rubber bag having walls of extremely high tensile strength capable of stretching several hundred percent and which was oblate in shape. The Board upheld the rejection based on the fact that the bag o the prior art is manipulated (filled, dropped, allowed to fall and a opened after impact) as claimed and that the structural differences of the bag do not alter these basic steps. In Leeson Corp. v. U.S., 185 USPQ 156, 165 (Ct. Cl. Trial div. 1975) aff’d 192 USPQ 672 (Ct. Cl. 1976) the claim was directed to a method of recharging a battery having a gas permeable nonconsumable envelope cathode in which the spent anode was removed from the nonconsumable envelope cathode and replaced with a fresh anode. The court stated that, in this case, it is apparent that the claimed method steps are not affected by the claimed cathode structure since the very same method would be used with the box cathode of Heise.” 185 USPQ at 165. The methods of recharging a battery “cannot be transformed into a patentably new one merely by using it to recharge a battery having cathode not shown in the prior art.” ID. At 165 (emphasis added).

2. **Regarding claim 2, Tong** discloses the method of claim 1, wherein providing comprises providing a fabrication substrate with at least one bond pad exposed at an active surface of each of the adjacent semiconductor device components (Tong, ¶ [0013] – interconnections – structural limitation do not have patentable weight – see regarding claim 1).

3. **Regarding claim 3, Tong** discloses the method of claim 2, wherein providing comprises providing a fabrication substrate with a plurality of semiconductor device components comprising at least one of semiconductor devices, interposers, and carrier substrates.

4. **Regarding claim 4, Tong** discloses the method of claim 2, wherein applying comprises applying the protective material such that the at least one bond pad of each of the plurality of semiconductor device components is exposed through the protective material sufficiently to effect electrical contact therewith (Tong, ¶ [0013]).

5. **Regarding claim 5, Tong** discloses the method of claim 2, wherein providing comprises providing the fabrication substrate with each of the plurality of semiconductor device components having a conductive structure protruding from the at least one bond pad thereof (Tong, ¶ [0013]).

6. **Regarding claim 6, Tong** discloses the method of claim 5, wherein applying comprises applying the protective material such that the protective material contacts a base portion of at least one conductive structure (Tong, ¶ [0013]).

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7. **Regarding claim 7, Tong** discloses the method of claim 6, wherein applying comprises forming a support structure around the base portion of the at least one conductive structure (Tong, ¶ [0013]).

8. **Regarding claim 8, Tong** discloses the method of claim 5, wherein applying comprises applying the protective material such that the protective material is spaced apart from a base portion of at least one conductive structure (Tong, ¶ [0013]).

19. **Regarding claim 19, Tong** discloses the method of claim 1, wherein applying comprises applying the protective material in a liquid state (Tong, ¶ [0013]).

20. **Regarding claim 20, Tong** discloses the method of claim 19, further comprising spreading the protective material to form a protective layer on the active surfaces (Tong, ¶ [0013]).

21. **Regarding claim 21, Tong** discloses the method of claim 20, wherein applying the protective material in the liquid state comprises applying a quantity of a substantially uncured polymer to the active surfaces (Tong, ¶ [0013]).

22. **Regarding claim 22, Tong** discloses the method of claim 21, further comprising partially curing the polymer prior to severing and at least partially severing (Tong, ¶ [0013]).

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23. **Regarding claim 23,** Tong discloses the method of claim 22, wherein healing is effected while the polymer remains in a partially cured state (Tong, ¶ [0013]).

24. **Regarding claim 24,** Tong discloses the method of claim 23, further comprising further curing the polymer following healing (Tong, ¶ [0013]).

25. **Regarding claim 25,** Tong discloses the method of claim 24, further comprising completely severing the adjacent semiconductor device components from one another along the street following healing (Tong, ¶ [0013]).

26. **Regarding claim 26,** Tong discloses the method of claim 20, wherein applying the protective material in the liquid state comprises applying liquefied thermoplastic material to the active surfaces (Tong, ¶ [0013]).

27. **Regarding claim 27,** Tong discloses the method of claim 26, further comprising permitting or causing the thermoplastic material to at least partially harden prior to severing and at least partially severing (Tong, ¶ [0013]).

28. **Regarding claim 28,** Tong discloses the method of claim 26, wherein healing comprises heating at least portions of the thermoplastic material located over peripheral regions of the adjacent semiconductor device components following severing and at least partially severing (Tong, ¶ [0013]).

29. **Regarding claim 29**, Tong discloses the method of claim 27, further comprising completely severing the adjacent semiconductor device components from one another along the street following healing (Tong, ¶ [0013]).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 9- 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. (US 2003/0171456) as applied to claims 1-8 above, and further in view of Glen et al. (US 6,650,019 A1).

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9. **Regarding claim 9, Tong** discloses the method of claim 1, however does not explicitly disclose wherein applying comprises applying a preformed sheet of protective material to the active surfaces (Tong, ¶ [0013]).

Glen et al. discloses at the time of the invention it was known in the art that the B-stageable material can be applied as preformed sheets (Glen, Col. 8 lines 36-58).

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Tong and Glen to enable the applying the B-stage material step of Tong to be performed according to the teachings of Glen because one of ordinary skill would have been motivated to look to alternative suitable methods of performing the disclosed application step of Tong and art recognized suitability for an intended purpose has been recognized to be motivation to combine.

MPEP 2144.07.

The spacer 50 can be made from a variety of materials, including a fiberglass matrix impregnated with a tacky, uncured (i.e., "B-stage") epoxy resin, or a ceramic, silicon or an oxide thereof, or alternatively, a plastic polymer sheet cut to the appropriate size. The adhesive layers 52 and 54 can be applied to the spacer 50 before it is attached to the first die 14, or alternatively, can be applied sequentially at the time the spacer is mounted to the die, first to the top surface of the first die 14, then to the top surface of the spacer before the second die is mounted on top of it. In yet another variation, the adhesive layer 54 used to mount the second die 16 on the spacer 50 can comprise the same adhesive material as the bead of uncured, fluid adhesive 40 dispensed around the perimeter 17 of the spacer 50, and can be deposited simultaneously therewith. In all cases, the layers of adhesive 52 and 54 on the spacer 50, and the layer 42 of adhesive 40 may all be simultaneously cured in a single step. (Glen, Col. 8 lines 36-58)

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10. **Regarding claim 10, Tong in view of Glen discloses the method of claim 9, wherein applying the preformed sheet comprises applying a preformed sheet comprising partially cured protective material (Glen, Col. 8 lines 36-58).**

11. **Regarding claim 11, Tong in view of Glen method of claim 9, wherein applying the preformed sheet comprises applying a preformed sheet comprising thermoplastic material.**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a thermoplastic material since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

12. **Regarding claim 12, Tong in view of Glen method of claim 9, wherein applying preformed sheet comprises applying a preformed sheet including apertures positioned to align with the at least one bond pad of each of the adjacent semiconductor device components (Tong, ¶ [0013]).**

13. **Regarding claim 13, Tong in view of Glen method of claim 2, wherein applying comprises applying a preformed sheet of protective material to the active surfaces (Glen, Col. 8 lines 36-58).**

14. **Regarding claim 14,** Tong in view of Glen method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet comprising partially cured protective material (Glen, Col. 8 lines 36-58).

15. **Regarding claim 15,** Tong in view of Glen method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet comprising thermoplastic material.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a thermoplastic material since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

16. **Regarding claim 16,** Tong in view of Glen method of claim 13, wherein applying the preformed sheet comprises applying a preformed sheet including apertures therein positioned to align with the at least one bond pad of each of the adjacent semiconductor device components (Tong, ¶ [0013]).

17. **Regarding claim 17,** Tong in view of Glen method of claim 13, wherein applying the preformed sheet comprises applying the preformed sheet such that a conductive

structure protruding from each of the adjacent semiconductor device components on the fabrication substrate passes through a plane of the preformed sheet (Tong, ¶ [0013]).

18. **Regarding claim 18**, Tong in view of Glen method of claim 17, further comprising heating each conductive structure prior to applying the preformed sheet (Tong, ¶ [0006]).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JJS  
January 12, 2007

  
MICHELLE ESTRADA  
PRIMARY EXAMINER